IIIT Allahabad
Office of Alumni Affairs

LIVE WEBINAR

Alumni Webinar Series #16 on

Topic: The Heartbeat of AI: From GPU Design to Silicon

Speaker

Mr. Arvind Vanam

Profile: Senior Manager – Core Graphics & AI Division @ Intel Corporation
B.Tech IT 2004 Batch

Chief Guest
Prof. Mukul S. Sutaone
Director IIITA

RSVP
Prof. Anupam
Dean (Alumni Affairs)

Wednesday

19th March. 2025

Time: 07:00 PM - 08:15 PM IST

Alumni Webinar Talk # 16 on 19th March. 2025 (07:00 PM to 08:15 PM IST)

Office of Alumni Affairs, IIITA, Prayagraj
Brief Biodata of the Speaker Mr. Arvind Vanam
(IIITA Alumnus, B. Tech. IT 2004 Batch, Enrollment No. B2004014)
Title of Talk: "The Heartbeat of AI: From GPU Design to Silicon"

Education

- B.Tech. (information Tech.) 2004 – 2008, IIIT Allahabad


Arvind Vanam

Professional Experience

Senior Manager – Graphics Hardware AI Division @ Intel Corporation | October 2020 – Present

- Leading 15+ engineers responsible for graphics IP config bring-up, design execution, and verification for Intel's Client Compute Group.
- Delivering Graphics IP to SoC for product builds across four generations of Intel's graphics architecture.
- Collaborated with architecture, RTL design, and validation teams to optimize GPU execution flows.

Co-Founder& Director @ Bodhileaf Technologies | November 2017 – June 2020

- Developed and executed end-to-end product development and manufacturing for hardware and IoT solutions.
- Designed and developed flagship products:
  - RAAHI – Asset tracking solution with GPS, GPRS, and WiFi.
  - VARUNA – Cloud-based water management system.
  - ZEUSBOX – LMS micro-server with integrated UPS and power management.
- Built Android applications, firmware for IoT devices, and backend cloud architecture.

Senior ASIC Engineer @ NVIDIA | May 2011 – June 2017

- Led hardware verification for Tegra series chips, with ownership on Audio Processing Engine, Security Engine, and Backbone Cluster.
- Developed testbenches, verification IPs, and test plans using SystemVerilog/UVM.
- Conducted FPGA prototyping and silicon bring-up, supporting software teams in driver development.
- Debugged and maintained RTL simulations, GLS, and X-Prop regressions.

Senior Software Engineer @ Cisco Systems | August 2008 – April 2011

- Developed firmware and software for Cisco's Edge Routers (C10K & ASR 9K).
- Implemented BGP PIC EDGE, punt filter debugging, and VPDN CLI/XML configurations.
- Worked on PXF (Forwarding Engine) components like QoS, Multilink (MLPPP, MLFR), and MPLS.
- Developed low-level firmware (Microcode for NT3PE) and high-level networking features in C.

Key Skills & Expertise

- Graphics IP Design & Execution
- Delivering Graphics IP to SoC for Product Builds
- ASIC & SoC Verification (Unit, Cluster, System-Level)
- FPGA Prototyping & Silicon Bring-up
- Hardware/Software Co-Verification
- Networking Software Development (QoS, MPLS, BGP, L2TP, Frame Relay)
- Firmware Development (Microcode, Assembly, C)
- UVM, SystemVerilog, RTL Design & Debugging
- IoT & Embedded Systems Development
- Cloud Computing (AWS, Google Cloud, MQTT, REST APIs)
- Android Development & Full-Stack Software Development